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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,599	08/30/2001	Gary L. Swoboda	TI-30481	2479
23494	7590	09/09/2005	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265				SAXENA, AKASH
		ART UNIT		PAPER NUMBER
		2128		

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/943,599	SWOBODA ET AL.
	Examiner	Art Unit
	Akash Saxena	2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 21 June 2005.
- 2a) This action is **FINAL**.      2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1,4,5,13,15,16,23,24 and 27-30 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1,4,5,13,15,16,23,24 and 27-30 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 30 August 2001 is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

**DETAILED ACTION**

1. Claims 1, 4, 5, 13, 15, 16, 23-24 & 27-30 have been presented for examination based on the amendment filed on 21<sup>st</sup> June 2005 for application 09/943599.
2. Claims 2-3, 6-12, 14, 17-22 and 25-26 are cancelled by the amendment.
3. Examiner withdraws objection to the specification for the missing "summary of Invention" based on its addition in the amendment.
4. Claim objections to claims 8 & 11 are moot and are withdrawn in view of their cancellation by the amendment.
5. Claim rejections under 35 USC 112 are also withdrawn in view of explanation provided in the amendment that there is only one trace stream. Further, rejection related to the "data processing operation" is also withdrawn and is understood as instruction execution.

***Response to applicant's arguments against Claim Rejections - 35 USC § 102***

6. Response to Arguments against Claim 1 rejection (Pg.18-20):

Applicant has argued that Mann (*Col.13 Lines 56-62*) does not teach “offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker.” Examiner agrees with the applicant, however the section pointed out above is to detail a situation where the offset would not be needed, i.e. data dependent disruptive events causing *direct program counter load*. Mann teaches (*Col.14 Lines 7-6*) that the instructions that do not cause disruption (non-data dependent conditional branches) will be included in the trace code (TCODE 1000, 0111 & 0001) with an offset and with the subsequent instructions with number of offset from the synchronization marker. As for the mention of the “number of program counter values”, It is inherent from the Mann’s teachings that the subsequent branch instruction address contents can be calculated from the base address (Mann: Col.14 – provided in TCODE 0010,0111 before the TCODE 0001 branching trace; Fig 6A,B) and each conditional branch will decide the subsequent number of counter values to be added to the base code. TCODE 0001 hold up to 15 subsequent trace branch conditions. Further, the synchronization marker is disclosed as TCODE entries 0010 & 0111, providing the complete base address for branch command (Table 6 & Col14 Lines 17-36).

Further, arguments relating to Col.15 Lines 8-15 state that the no teaching to synchronization marker being the same as the segment base address. Mann

teaches that each synchronization event (TCODE command) provides address information and it is clear from Table 6 that base address is provided as part of the synchronization (all TCODES except TCODE 0001). Further, the claims as disclosed do not differentiate between segment base address and complete program counter address. Examiner respectfully finds the applicant's arguments them unpersuasive. Further, examiner would points out that the Mann reference should be considered in its entirety as teaching/anticipating the proposed claim.

7. Response to Arguments against Claims 4 & 5 rejection (Pg. 20-21):

Examiner agrees with the argument made by the applicant and withdraws the rejection.

However, It would still be inherent from Mann's teachings to identify the loading of the program counter (to reset the TSYNCH register value as noted earlier), this time to keep for the purpose of code coverage, execution performance and performance tuning (Col.16 Lines 61-64). Further, the functional need to keep count of the number of loads and offset value is to be able to compress the data transmitted when program counter is referenced against the memory (Specification: Pg.30 Lines 16 onwards). Handling the conditional branches in a single TCODE command and providing complete program counter address, addresses this functional need.

Please see further 35 USC 103 rejections.

8. Response to Arguments against Claim 13 rejection (Pg. 22):

Applicant argues that Mann fails to teach synchronization marker or offset recited in claim 13. Mann teaches the synchronization marker as TCODE (Table 6; Col.

16Lines 13 – 16) where all TCODE (except TCODE=1) act as synchronization marker providing the updated address information. Further, Mann teaches program counter values as offset, where TCODE=1 branch statement contains subsequent branch statements with offsets for program counter based if the branch was taken (Col.14 Lines 7-36). Further, applicant argues that Mann teaches trace address values are an offset with a segment base address. There is no limitation in the claims that offset cannot be an offset from the case segment base address when the segment base address is loaded in as part of program counter content. Hence the argument is mute in light of claim 13. Further, applicant argues that there is no teaching that a synchronization marker is the same as segment base address. Examiner would like to point out again that there is no limitation in the claims as understood by the examiner that precludes segment base address as being the base address. Further, as stated above, Mann teaches that all synchronization events except TCODE=1 provide address information. Further not all TCODE provide segment base address. Some of them (Table 6; Fig 6C; TCODE=6, 7 & 8) are specifically designed to provide trace synchronization whenever tracing is stopped or started. Further applicant argues that Mann fails to teach that trace address values following the synchronization marker are offset from the synchronization marker value. On the contrary Mann teaches that future trace value are calculated based on known program target address and then the conditional branch statements (TCODE=1) are followed by for correct program flow tracing (Col.15 Lines 42-52):

When executing typical software on a processor-based device 102 according to the disclosed embodiment of the invention, few trace entries contain address values. Most entries are of the TCODE=0001 format, in which a single bit indicates the result of a conditional operation. When examining a trace stream, however, data can only be studied in relation to a known program address. For example, starting with the oldest entry in the trace cache 200, all entries until an address entry are of little use. Algorithm synchronization typically begins from a trace entry providing a target address.

Examiner respectfully disagrees with the applicant's argument and finds it unpersuasive.

9. Response to Arguments against Claims 15 & 16 rejection (Pg. 22-23):

Examiner respectfully disagrees with the applicant's argument and finds it unpersuasive for the same reasons as stated in claim 13 responses above. Please see further for the 35 USC 103 rejections related to amended claims.

10. Response to Arguments against Claim 23 & 24 rejection (Pg. 22-23):

Claim 23 & 24 disclose integrated circuit & data processing system embodiments having same limitations as claim 13. Applicant argues that examiner response to combine Sites, Mann and Edwards does not make obvious the subject matter present in claim 23 & 24. Examiner agrees with the applicant that claim 13 alone does not teach the limitations of claim 23 & 24, but the limitations of the 23 and 24 substantially recite the same limitation as claim 13-15 in old claim set. All the arguments relating to synchronization marker and offset are addressed in the claim 13 and 15-16 arguments above. Further, applicant argues that the office action does not allege that Sites or Edwards adds any teaching to Mann; Examiner respectfully disagrees. Sites teaches the integrated circuit (apparatus) performing a tracing and Edwards teaches non-intrusive tracing and compression of trace. Both the references are analogous art to Mann and further teach Mann various embodiments

(apparatus & system) and compression techniques. For example Edwards teaches PC counter compression by sending the offset for the program counter in various formats (Edwards: Col.18 Lines 44 onwards, Fig 11A-B). Further, please see the clarified 35 USC 103 rejections below for the substantially similar limitations presented in claim 15.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**11. Claims 1,4,5 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S.**

**Patent No 6,009,270 issued to Daniel Mann '270 (Mann '270 '270 hereafter).**

**Regarding Claim 1**

Amended claim 1 states "...providing trace information indicative of a each processing operation...". Claim 1 rejection based on Mann '270 is disclosed in previous office action and is included here by reference. Further, arguments provided above also apply here to clarify the claim rejection. Mann '270 teaches providing trace information indicative of the instruction execution flow, which includes all processing operations (Col.2 Lines 60 – Col.3 Lines 30; Especially Col.2 Lines 21-23).

**Regarding Claim 4**

The amended claim 4 amends the limitations of claim 3. Mann '270 clearly teaches that conditional branching statements (TCODE=1) are relevant only after the some base address (complete PC address) is provided by other TCODE instructions (Col.15 Lines 42-52; Col.16, Lines 13-15). Further, in the conditional branching

statement a new program counter is loaded based on if the branch is taken, each branch will lead to new value in PC, hence detecting a new branch will inherently mean detecting occurrences program counter load.

Further, Mann '270 teaches identifying step to include counting detected occurrences of program counter load as follows. Each bit in the trace command (TCODE=1) represents a single program counter load; hence the number of bits used (up to 15) in the trace command will indicate the number of program counter loads. The trace command besides storing the decision for branch also acts as a counter of how many program counter loads have taken place (Table 6; Col.14 Lines 7-36).

Regarding Claim 5

Claim 5 inherits all its limitation from claim 4, thus rejection presented above also pertains to claim 5 above. Further, claim 5 discloses maintaining a running count of number of program counter loads. Mann '270 teaches, as disclosed above, a running count as number of bits in the TCODE=1 statement, that have occurred after the insertion of the synchronization marker (all TCODE statements except TCODE=1) (Table 6; Col.15 Lines 42-52).

***Claim Rejections for Amended/New - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**12. Claims 13,15 & 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,764,885 issued to Richard L. Sites et al (Sites '885 hereafter) in view of U.S. Patent No. 6,009,270 issued to Daniel Mann (Mann '270 hereafter).**

Regarding Claim 13

Claim 13 rejection based on Sites '885 and Mann '270 '270 is disclosed in previous office action and is included here by reference. Further, arguments provided above also apply here to clarify the claim rejection.

Regarding Claim 15

The new claim 15 amends in the limitations of claim 14. Mann '270 clearly teaches that conditional branching statements (TCODE=1) are relevant only after the some base address (complete PC address) is provided by other TCODE instructions (Col.15 Lines 42-52; Col.16, Lines 13-15). Further, in the conditional branching statement a new program counter is loaded based on if the branch is taken, each branch will lead to new value in PC, hence detecting a new branch will inherently mean detecting occurrences program counter load.

Further, Mann '270 teaches identifying step to include counting detected occurrences of program counter load as follows. Each bit in the trace command (TCODE=1) represents a single program counter load; hence the number of bits used (up to 15) in the trace command will indicate the number of program counter loads. The trace command besides storing the decision for branch also acts as a

counter of how many program counter loads have taken place (Table 6; Col.14 Lines 7-36).

Regarding Claim 16

Claim 16 inherits all its limitation from claim 15, thus rejection presented above also pertains to claim 15 above. Further, claim 15 discloses maintaining a running count of number of program counter loads. Mann '270 teaches, as disclosed above, a running count as number of bits in the TCODE=1 statement, that have occurred after the insertion of the synchronization marker (all TCODE statements except TCODE=1) (Table 6; Col.15 Lines 42-52).

**13. Claims 23-24 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,764,885 issued to Richard L. Sites et al (Sites '885 hereafter) in view of U.S. Patent No. 6,009,270 issued to Daniel Mann (Mann '270 hereafter), further in view of U.S. Patent No. 6,732,307 issued to David A. Edwards (Edwards '307 hereafter).**

Regarding Claims 23 & 24

Claim 23 & 24 rejection based on Sites '885, Edwards '307 & Mann '270 disclosed in previous office action and is included here by reference. Further, responses to arguments provided above also apply here to clarify the claim rejection.

Regarding Claims 27 & 29

Claims 27 and 29 disclose substantially similar limitation for an integrated circuit and a data processing system. Mann '270 clearly teaches that conditional branching statements (TCODE=1) are relevant only after the some base address (complete PC

address) is provided by other TCODE instructions (Col.15 Lines 42-52; Col.16, Lines 13-15). Further, in the conditional branching statement a new program counter is loaded based on if the branch is taken, each branch will lead to new value in PC, hence detecting a new branch will inherently mean detecting occurrences program counter load.

Further, Mann '270 teaches identifying step to include counting detected occurrences of program counter load as follows. Each bit in the trace command (TCODE=1) represents a single program counter load; hence the number of bits used (up to 15) in the trace command will indicate the number of program counter loads. The trace command besides storing the decision for branch also acts as a counter of how many program counter loads have taken place (Table 6; Col.14 Lines 7-36).

#### Regarding Claims 28 & 30

Claims 28 & 30 inherit their limitation from claims 27 and 29 respectively, thus rejection presented above also applies here. Claim 27 & 29 discloses maintaining a running count of number of program counter loads. Mann '270 teaches, as disclosed above, a running count as number of bits in the TCODE=1 statement, that have occurred after the insertion of the synchronization marker (all TCODE statements except TCODE=1) (Table 6; Col.15 Lines 42-52).

**Conclusion**

14. All claims 1, 4, 5, 13, 15, 16, 23-24 & 27-30 are rejected.

15. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant.

Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R. Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Akash Saxena  
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Wednesday, August 24, 2005

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